Characterization of the Oxide-Semiconductor Interface in NO, P, and N-Plasma Passivated *4H*-SiC/SiO$_2$ Structures Using TEM

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8th Annual SiC MOS Workshop ("SiC Device Review")
University of Maryland, College Park
Thursday, August 22, 2013 – 2:00PM

*Supported by ARL under contract no. W911NF-11-2-0044 and W911NF-07-2-0046.

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[3] Institute for Advanced Materials, Rutgers University
[4] U.S. Army Research Laboratory

THE DEPARTMENT *of*
MATERIALS SCIENCE AND ENGINEERING

Motivation and background

- SiC: Very promising for high temperature, high power, and high radiation environments
  - MOSFET devices limited by poor channel carrier mobility and reliability
  - Best device μ_{FE}: SiC ~ $125\ \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}}$ (a-face P passivation)[◊]; Si ~ $600\ \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}}$ (uniaxial <100> strain)[⟠]
  - Electrically active defects at the SiC/SiO_2 interface inhibit devices during channel inversion
- How to passivate these defects and improve mobility?
  - Incorporation of N at interface
    - NO anneal – improves μ, but can introduce additional defects[†]
    - N-plasma anneal – incorporates N without additional oxidation[⊖]
  - Incorporation of P at interface
    - Anneal in P_2O_5 – P dopants have lower activation energy than N[⊗]
  - N and P passivate dangling bonds/modify interface

[◊] G. Liu *et al.*, IEEE Electron. Dev. Lett. **34**, 181–183 (2013).

[⟠] K. Uchida *et al.*, IEDM Tech. Dig. 229-232 (2004).

[†] J. Rozen, in *Physics and Technology of Silicon Carbide Devices* (InTech, 2012), pp. 251–278.

[⊖] X. Zhu *et al.*, Solid-State Electron. **57**, 76–79 (2011).

[⊗] Y. Sharma *et al.*, Solid-State Electron. **68**, 103–107 (2012).

Central questions

How do the structure and chemistry of the 4H-SiC/SiO_2 interface change under various processing conditions?

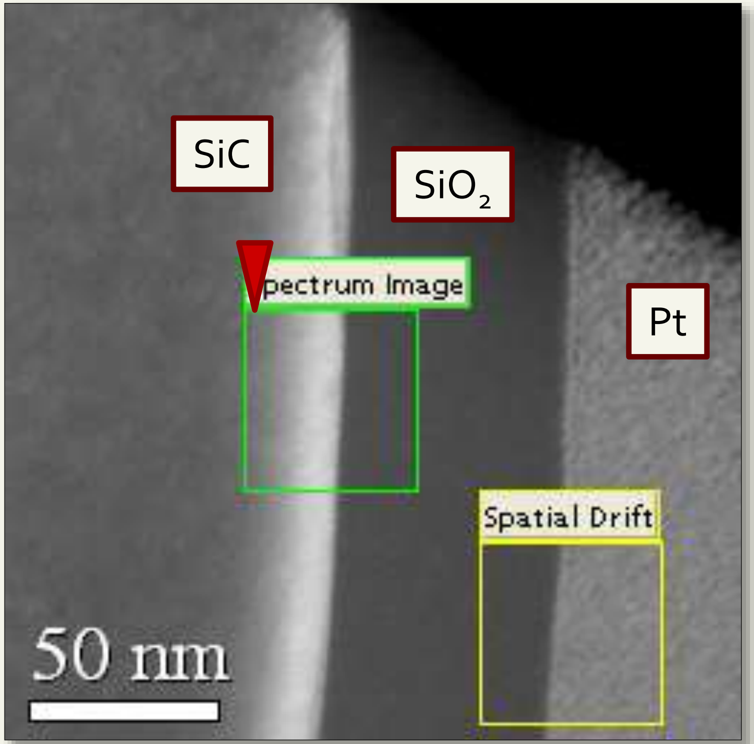
What do these changes tell us about the effects of these passivation processes?

Outline

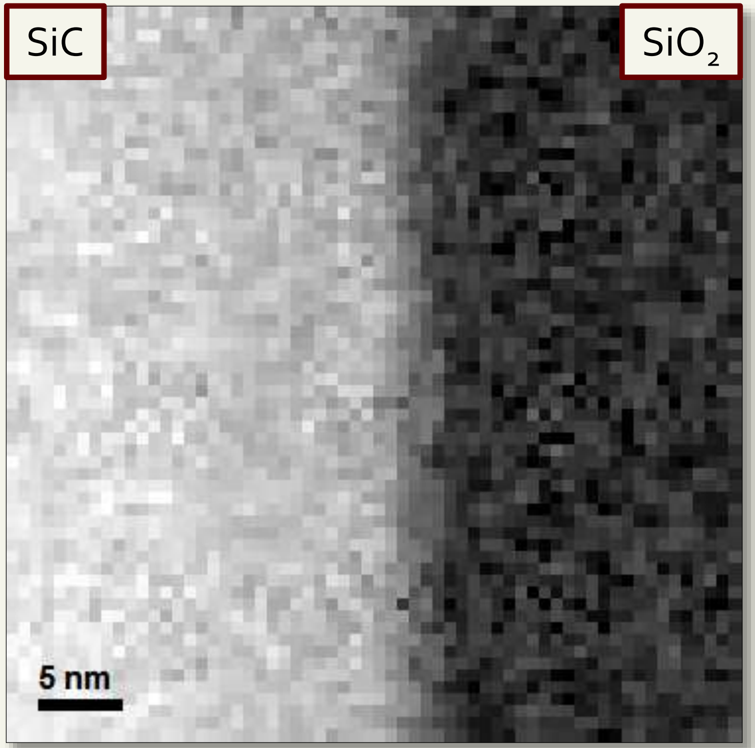
- Background/Review of prior work and methods
  - Characterization of transition layer in NO-annealed *4H*-SiC MOSFETs
    - J. Taillon *et al.*, *J. Appl. Phys.* 113, 044517 (2013).
    - Transition layer width compared to electronic properties
- Recent work
  - Comparison of NO-annealed samples with P and N-plasma passivated *4H*-SiC devices
    - Refinement of experimental methods
    - Comparison of *a*-face and Si/C-face devices
    - Comparison and analysis of passivation methods
    - Analysis of time dependence in N_2P passivation
- Future areas of inquiry
  - TEM investigation of interfacial roughness
  - XPS depth profiles and correlation with EELS fine structure

BACKGROUND/PRIOR WORK

Spectrum Imaging

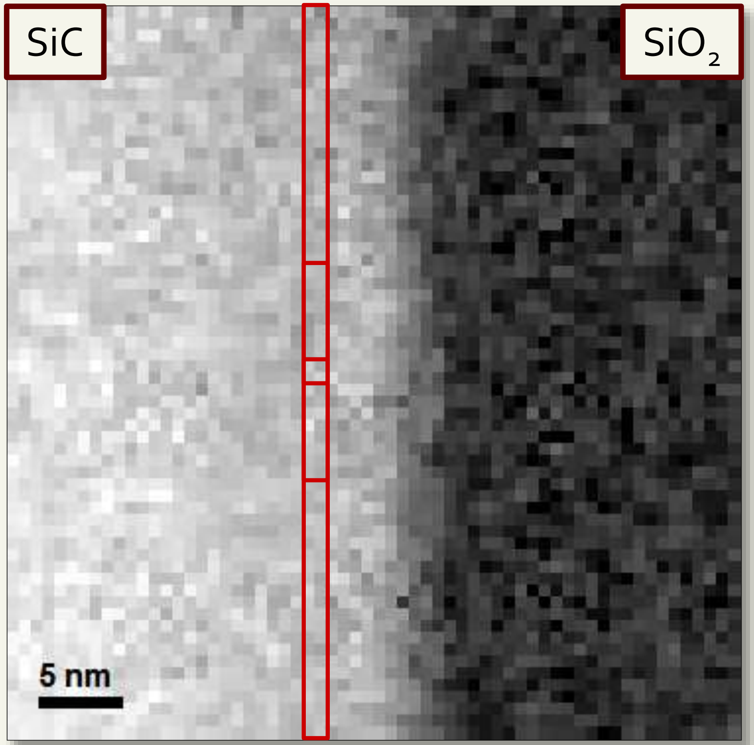


HAADF Image
(60 minute NO anneal)

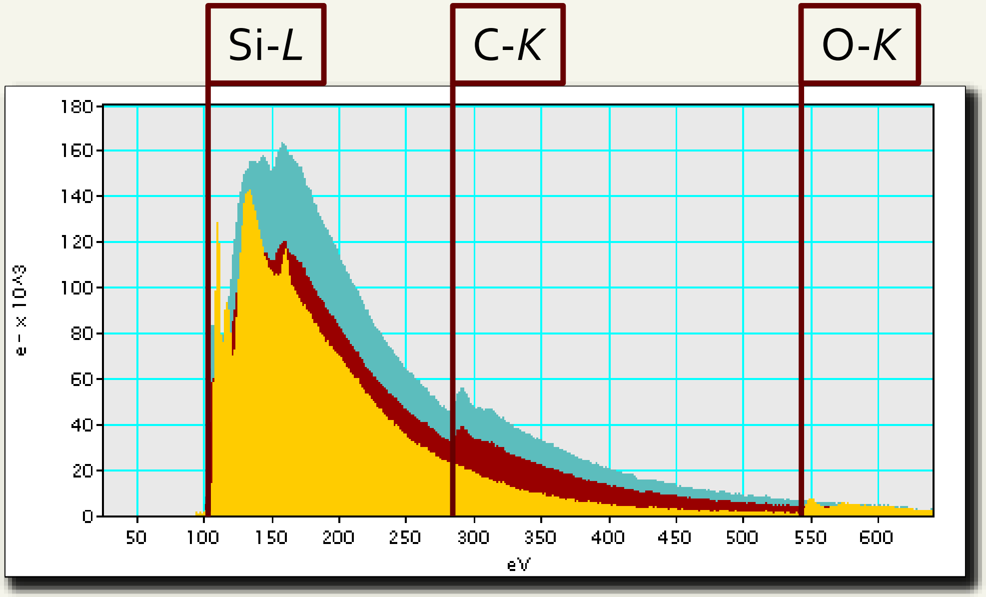


Spectrum Image
(60 minute NO anneal)

Spectrum imaging



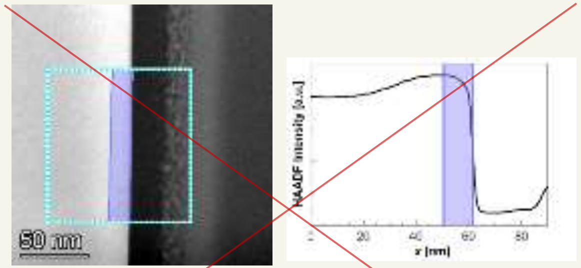
Spectrum Image
(60 minute NO anneal)



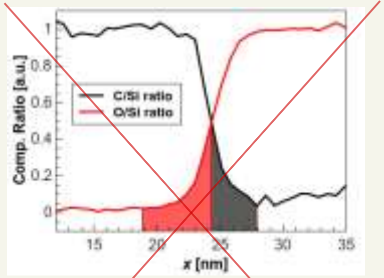
Background-subtracted spectrum
(60 minute NO anneal)

Transition layer width measures

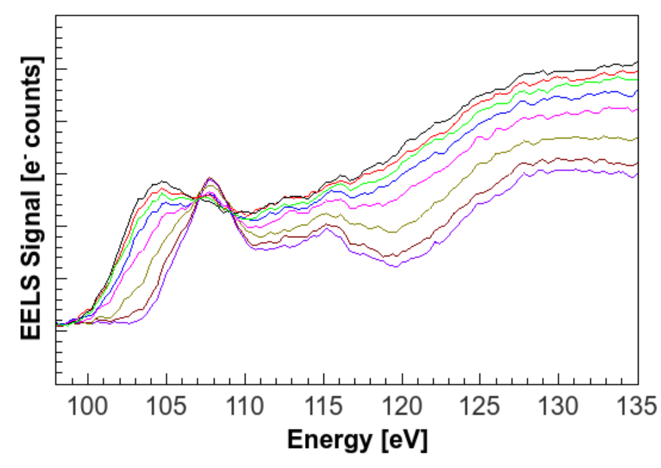
- Using electron energy loss spectroscopy (EELS) along with high-angle annular dark field (HAADF) imaging within a transmission electron microscope (TEM)



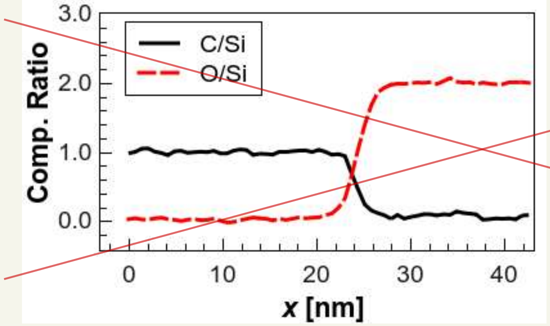
~~HAADF intensity profiles~~



~~Elemental inter-diffusion profiles~~

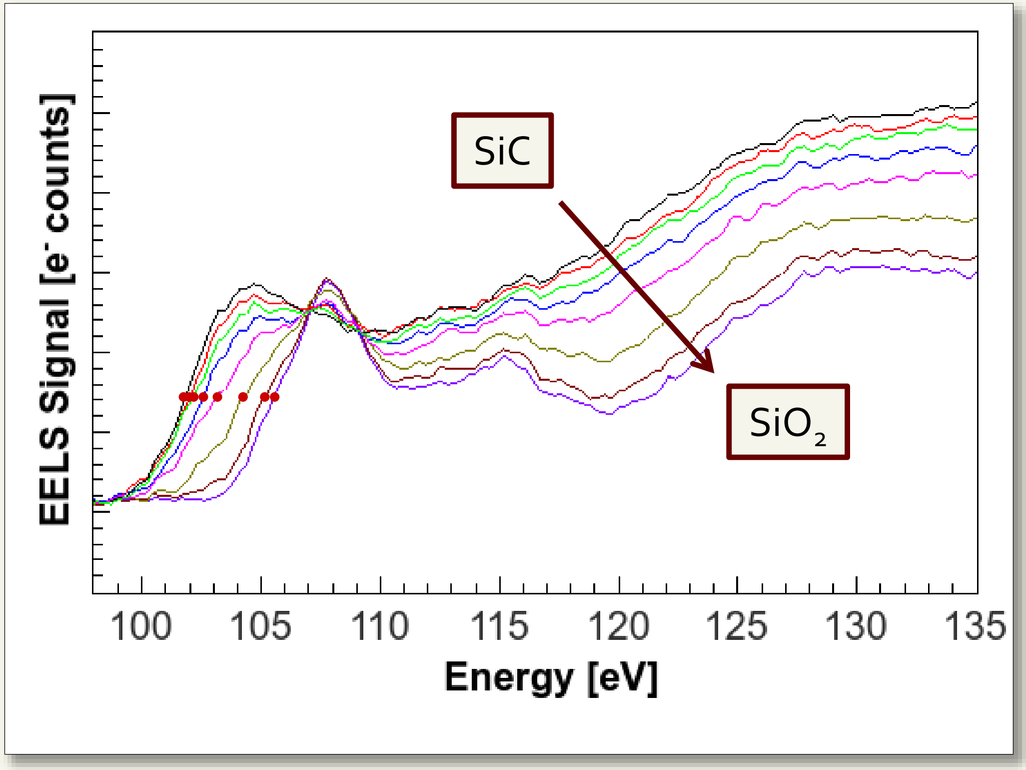


Si $L_{2,3}$ edge chemical shift



~~Elemental composition ratios~~

Si-$L_{2,3}$ chemical shift



- EELS fine structure (ELNES) reflects local unoccupied density of states
  - Semiconductor → insulator
  - Edge onset → minimum energy needed to excite core shell e^-
  - Band gap widens, core levels depressed relative to E_F[1]
    - Charge transfer from Si → C/O
    - Onset shifts to higher energy

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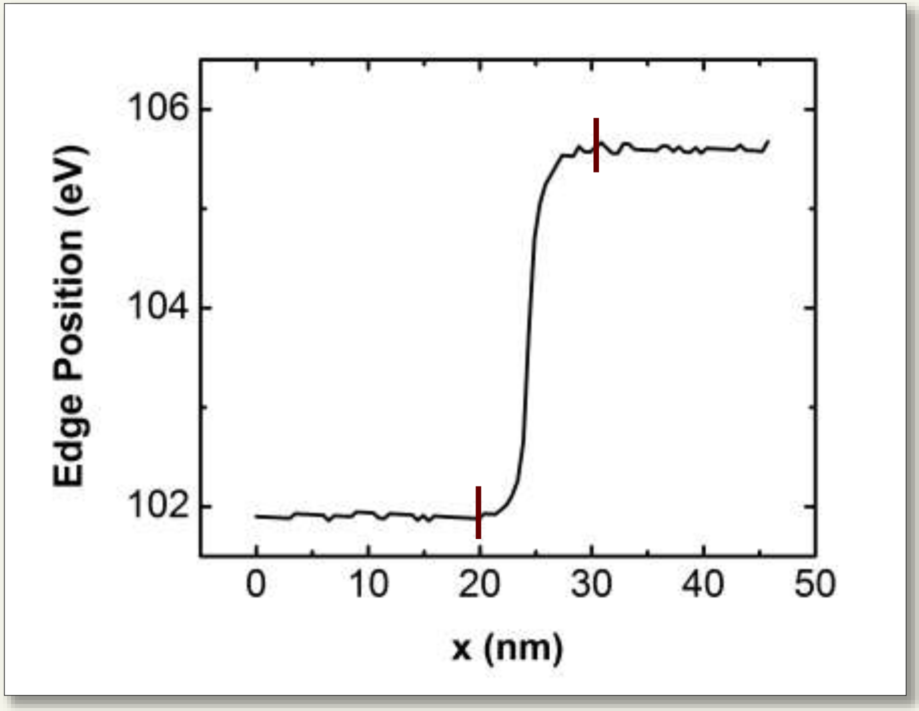
[1] D. Muller, Ultramicroscopy **78**, 163 (1999).

Si-$L_{2,3}$ chemical shift

- Track inflection point of edge onset across interface[1]
- Gradual and monotonic shift
  - Si bonding changes gradually and uniformly across the interface



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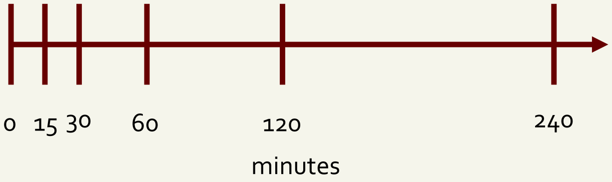
[1] D. Muller, P. Batson, and J. Silcox, Physical Review B **58**, 11970 (1998).

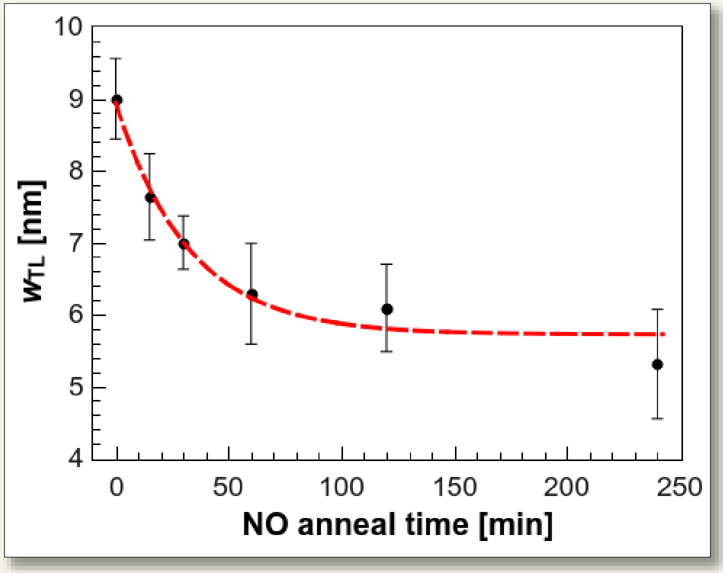
NO-anneal samples

- Six SiC/SiO$_2$ samples: 0-240 minutes of NO-anneal



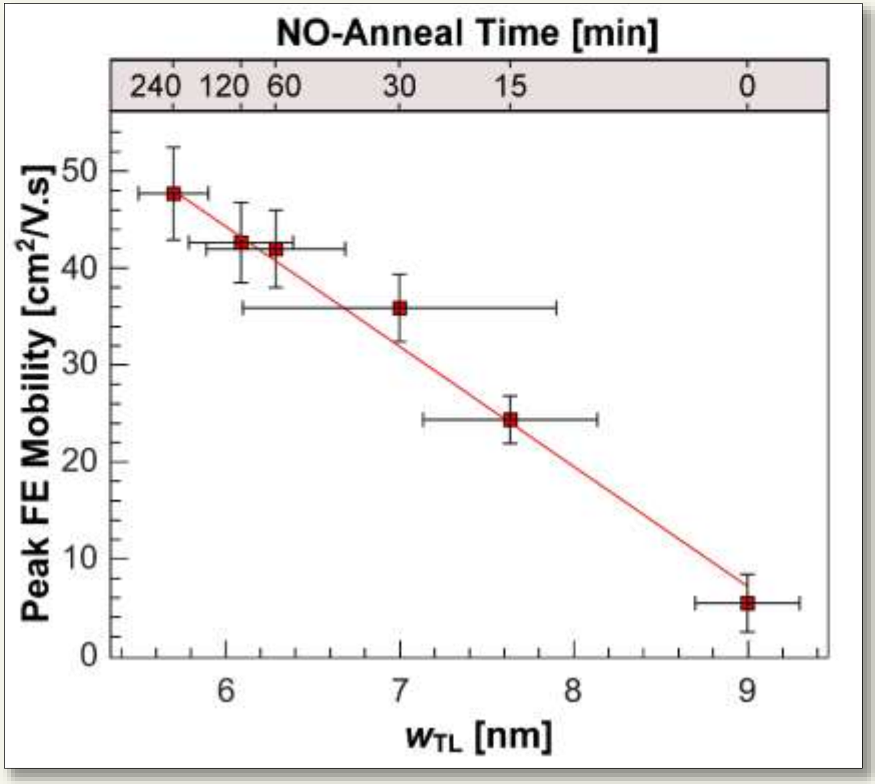
  - 150 μm n-channel MOSFET devices
  - deposited epitaxial layer ($N \approx 5 \times 10^{15}$ cm^{-3})
  - (0001) 4° miscut wafers from Cree, Inc.
  - Cross-sections from gate region of devices

- Significant NO anneal improvement
  - Best method to track transition layer
  - (Relatively) insensitive to spectral noise
- Characterizes bonding instead of composition



NO-anneal results

- w_{TL} correlates inverse-linearly μ_{FE}
  - Confirming previous work results by Biggerstaff *et al.* with systematic samples
- NO-anneal removes/passivates mobility-limiting defects
  - Compositionally and electronically
- **Conclusions:**
  - w_{TL} decreases with increasing NO anneal time
    - New chemical shift of Si-$L_{2,3}$ edge onset was most reliable method
    - No excess C on either side of interface



J. Taillon, L. Salamanca-Riba, *et al.*, *J. Appl. Phys.* 113, 044517 (2013).

RECENT WORK

Method refinements

- Optimization of EELS-SI collection
  - Each data set is equivalent to ~250 line scans
  - Compared to single line scans/small SI from last year
- Development of scripts to automate and improve data processing
- Redefined extent of transition layer
  - Using 98%/2% definition as suggested by Williams and Carter
  - This definition includes contributions from 90% of electrons

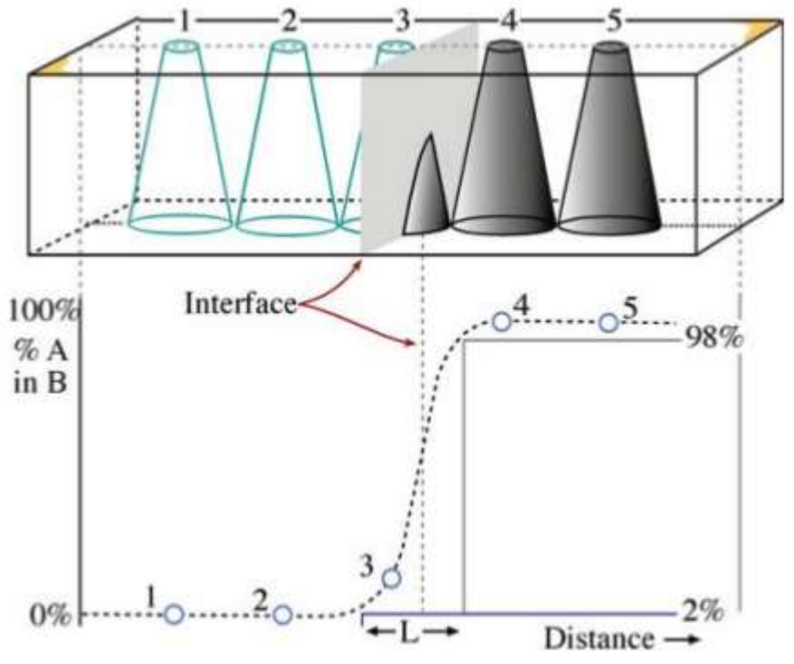
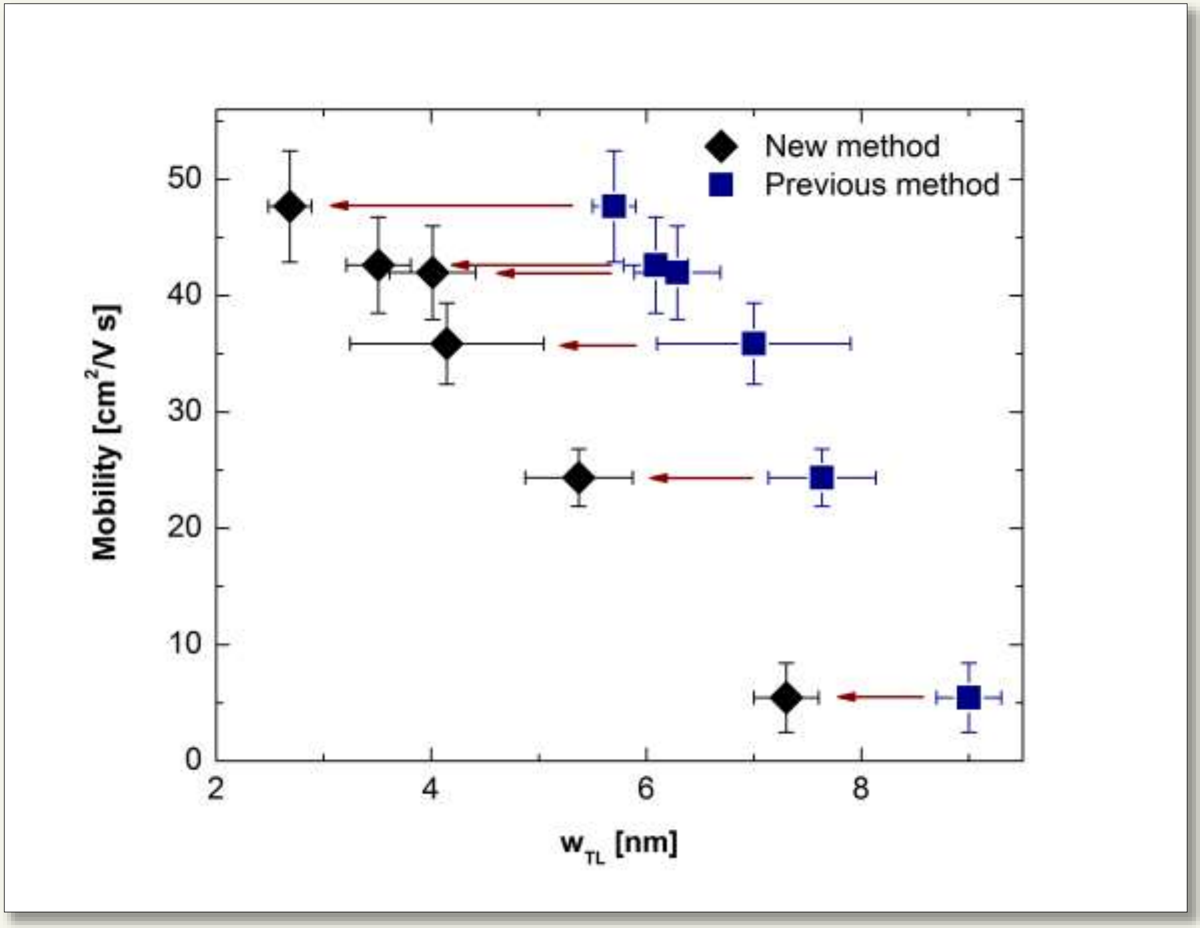


FIGURE 36.4. Schematic diagram showing a composition profile measured across an interface at which an atomically discrete composition change occurs (like the simulation in Figure 36.2). The measured spatial resolution can be defined in terms of the extent (L) of the measured profile between the 2% and 98% points.

Williams and Carter (2009), p. 667

Method refinements



NO-anneal data from 2012

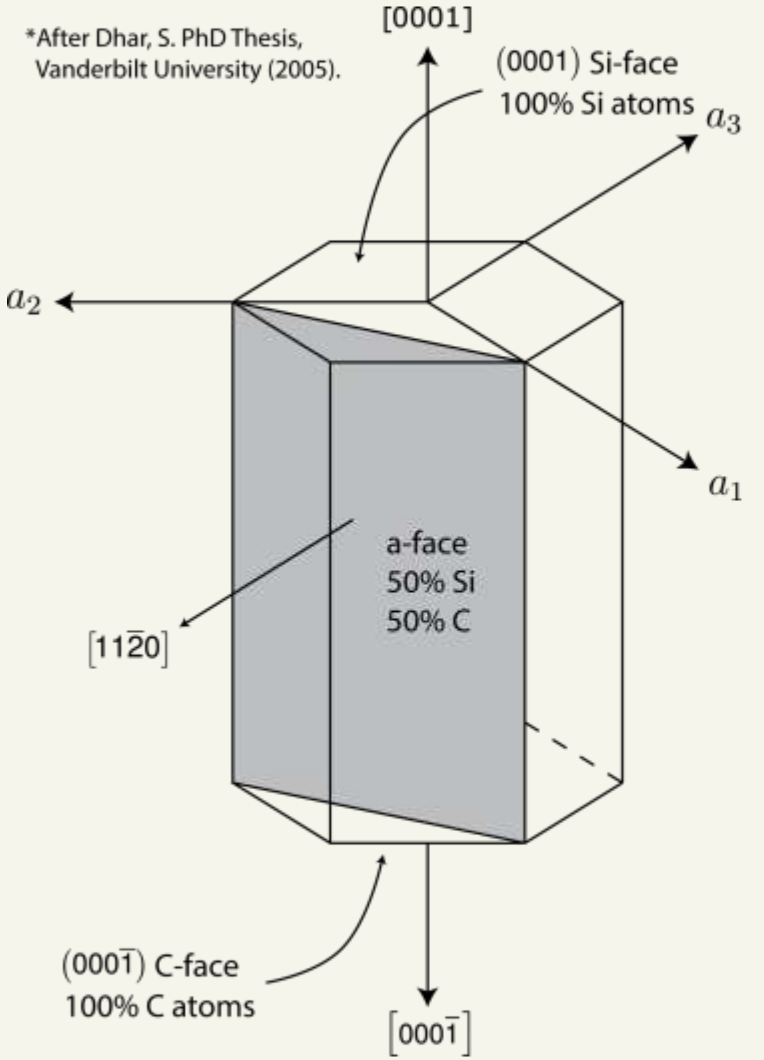
Smaller w_{TL} values, but same trend

Recent work

Process / Face	NO	P	N2P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
***a* - $(11\bar{2}0)$**	2 hrs	4 hrs	X
C - $(000\bar{1})$	2 hrs	X	X

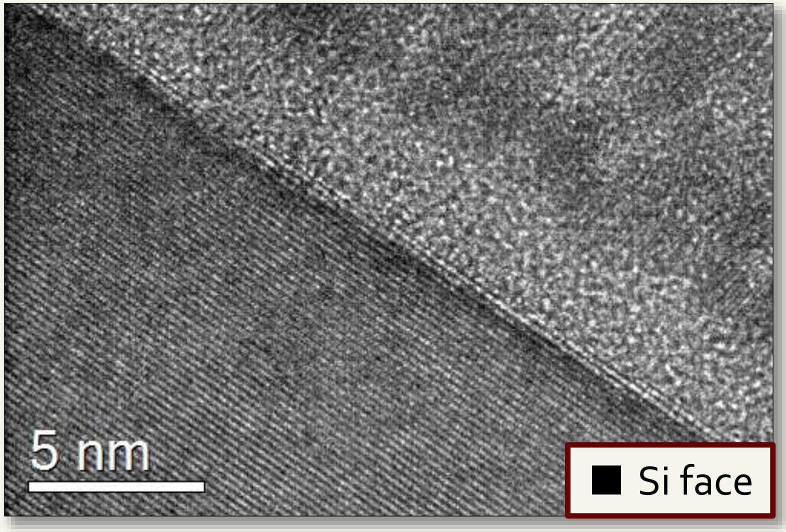
Miscut on Si and C faces:
4° or 8°

No miscut on *a* face

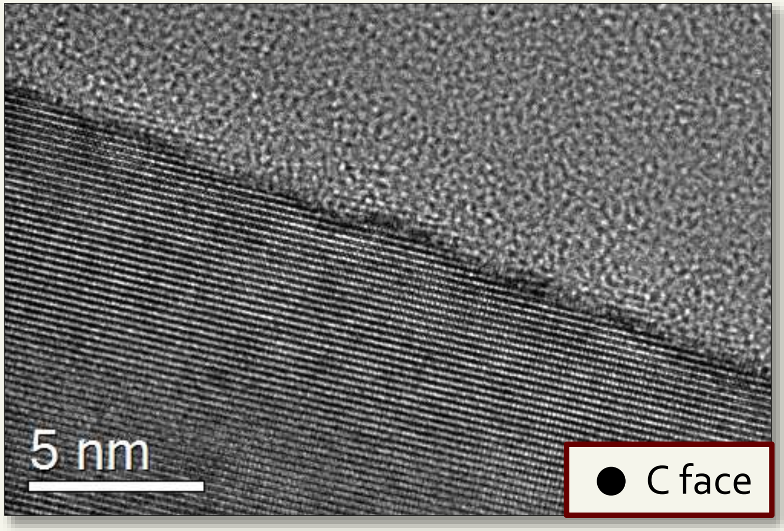


*After Dhar, S. PhD Thesis, Vanderbilt University (2005).

NO anneal

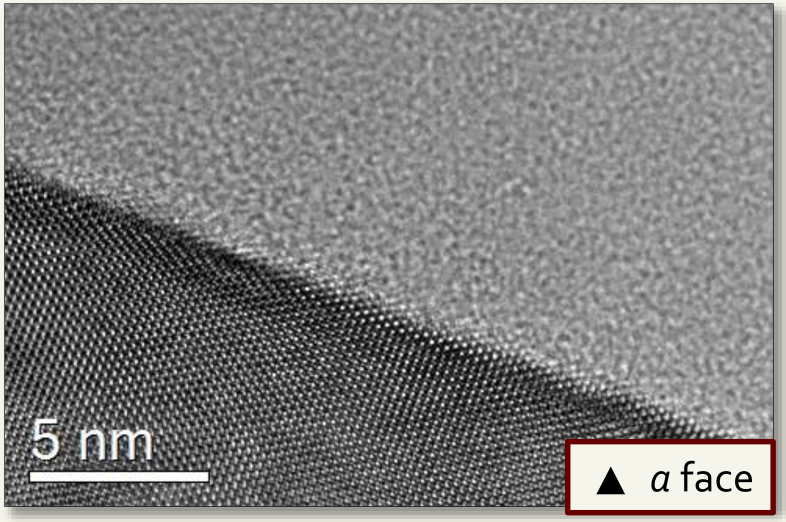


Si face device appears much like NO-samples analyzed previously with 4° miscut evident

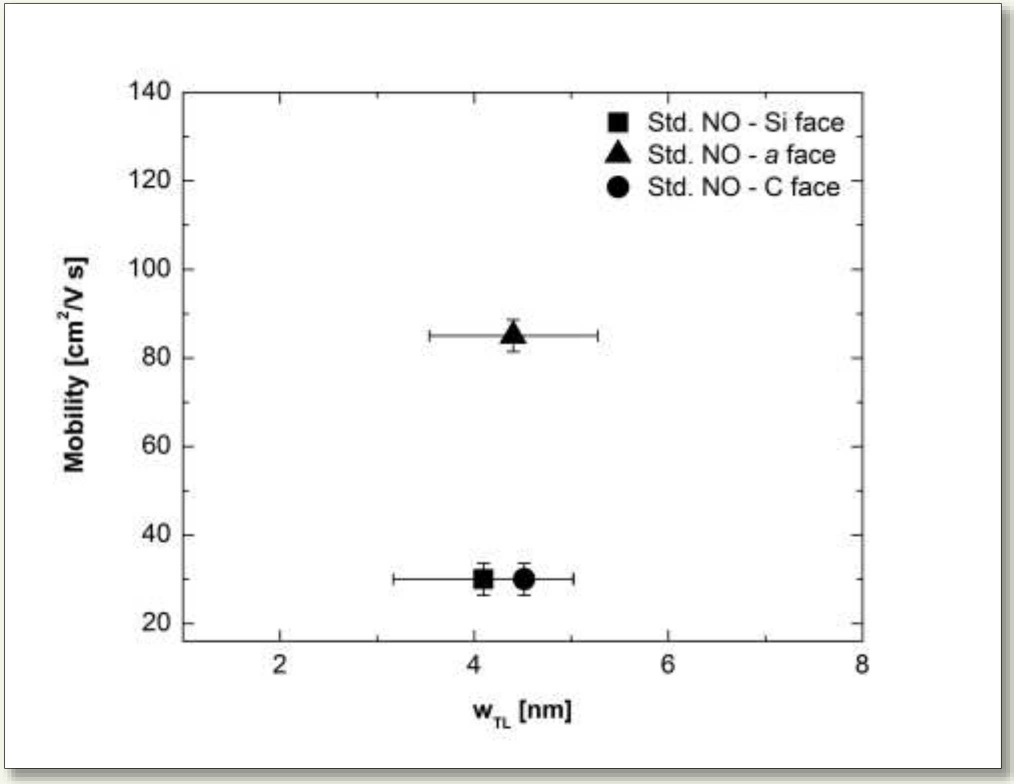


C face device is 8° miscut, giving greater roughness (larger than steps); does this affect properties?

NO anneal



a face device has *very* flat interface

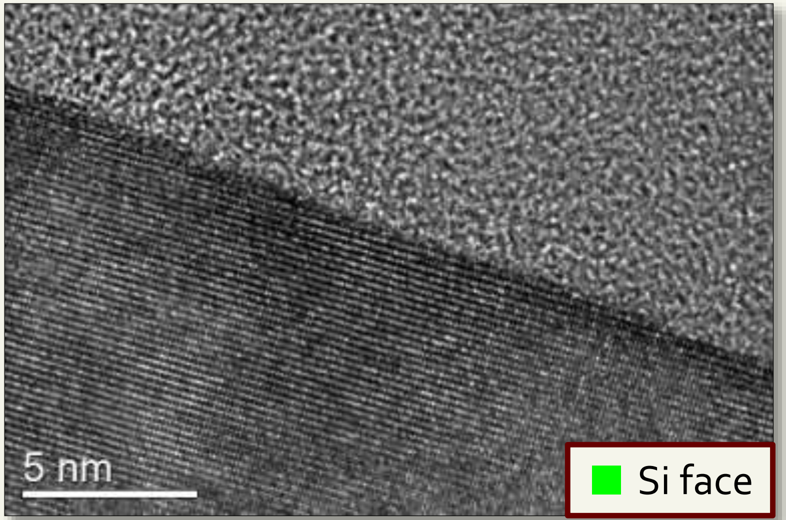


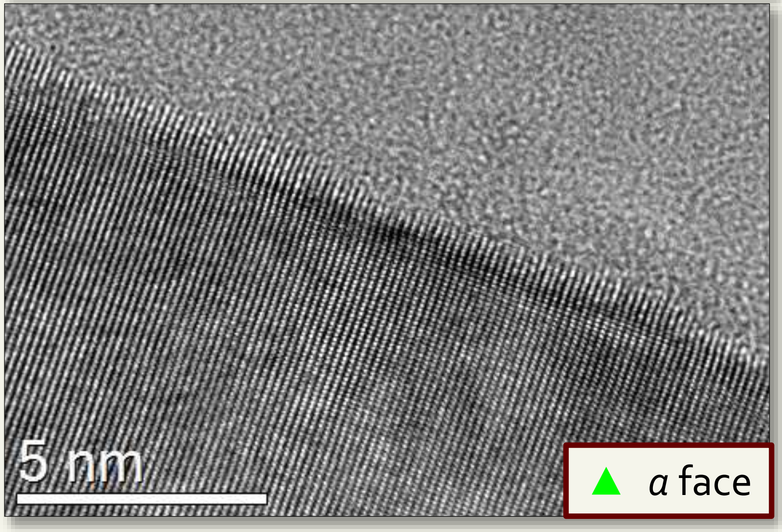
- Identical w_{TL} regardless of device face
  - All samples annealed for 2 hours
- Mobility improvement observed for *a*-face
- Indicates influence of another factor on mobility, besides just w_{TL}
- Roughness of C-face sample does not seem to have large effect
- Thin oxide in Si-face sample does not seem to have significant effect

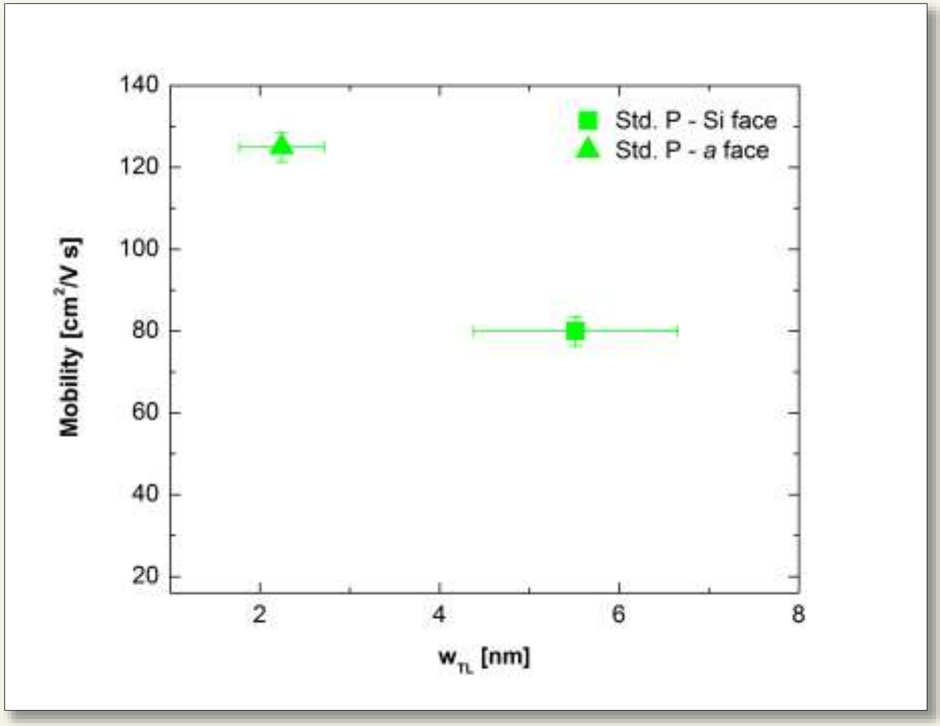
Recent work

Device Process / Crystal face	NO	P	N2P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
a - $(11\bar{2}0)$	2 hrs	4 hrs	X
C - $(000\bar{1})$	2 hrs	X	X

P anneal



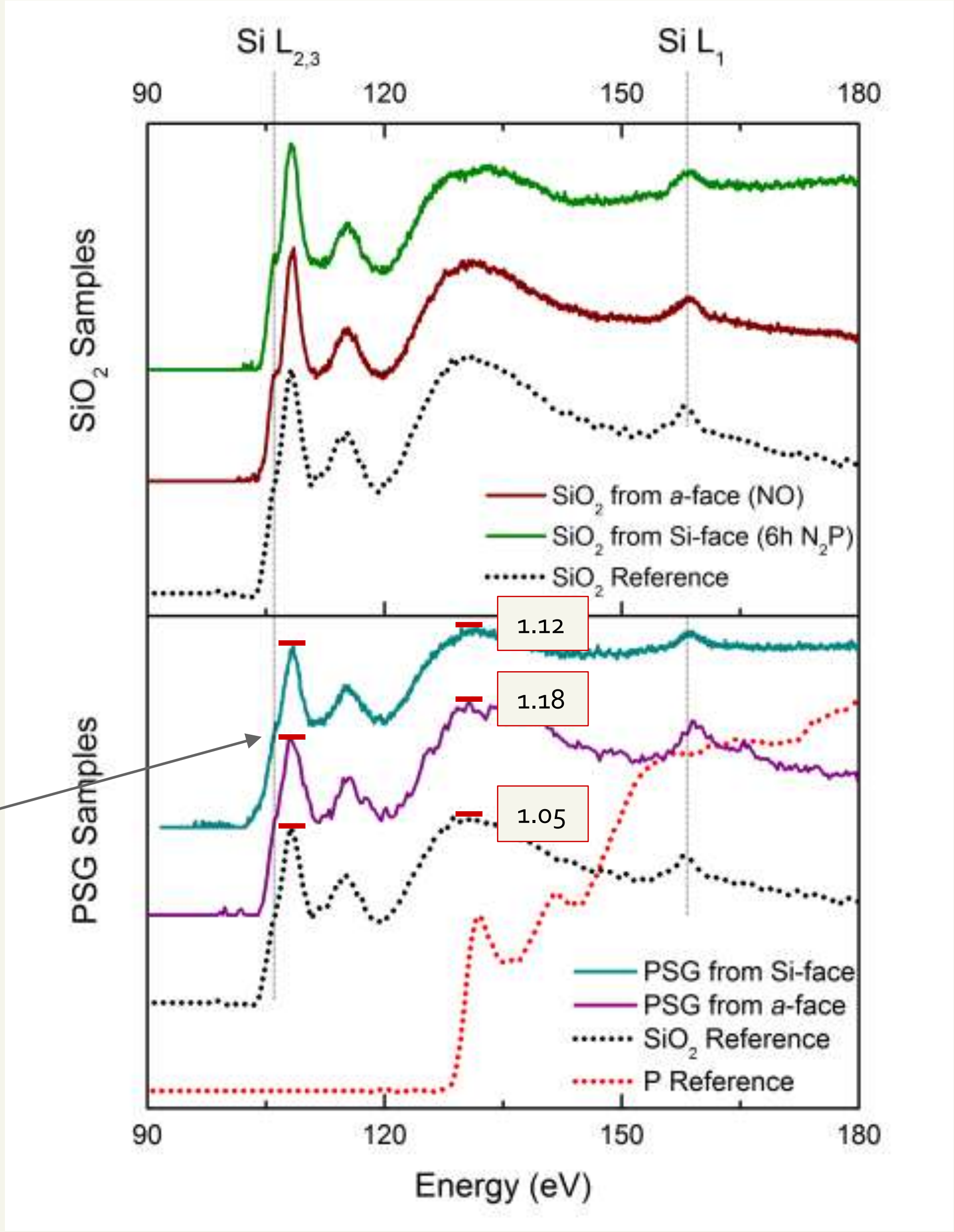




- HRTEM images do not reveal obvious reason for mobility enhancement
- Observation of expected w_{TL} "trend" (only two samples)

PSG compared to SiO_2

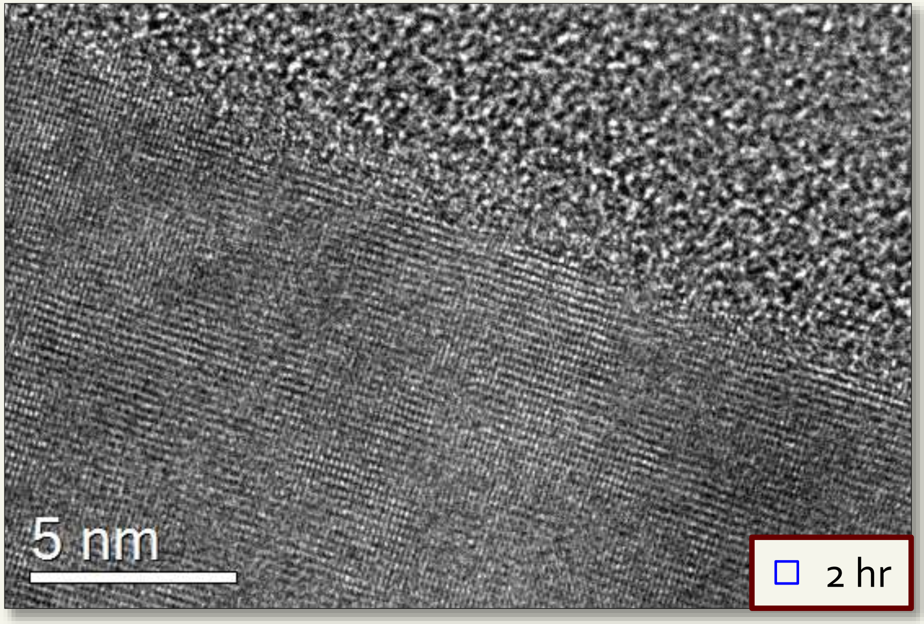
- Spectra from NO and N_2P samples all well matched to SiO_2 reference
- Spectra from P-annealed samples also well matched to SiO_2 reference, with some variance
  - Very little EELS evidence of P within oxide, but:
  - Ratio of Si $L_{2,3}$ ELNES changes in PSG
- Cannot quantify P signal due to edge overlap, but does alter electronic response within specimen



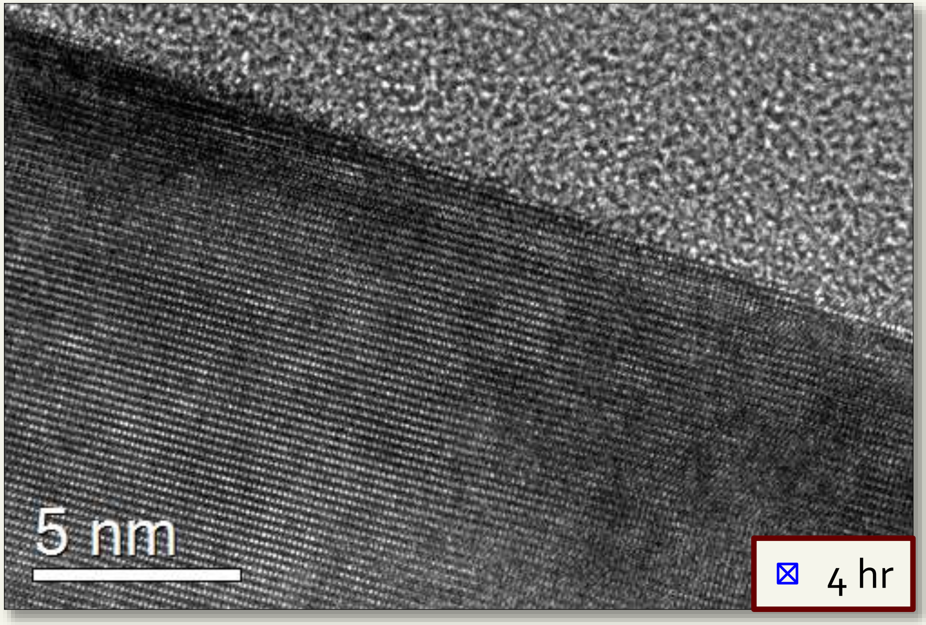
Recent work

Device Process / Crystal face	NO	P	N2P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
a - $(11\bar{2}0)$	2 hrs	4 hrs	X
C - $(000\bar{1})$	2 hrs	X	X

N$_2$P anneal

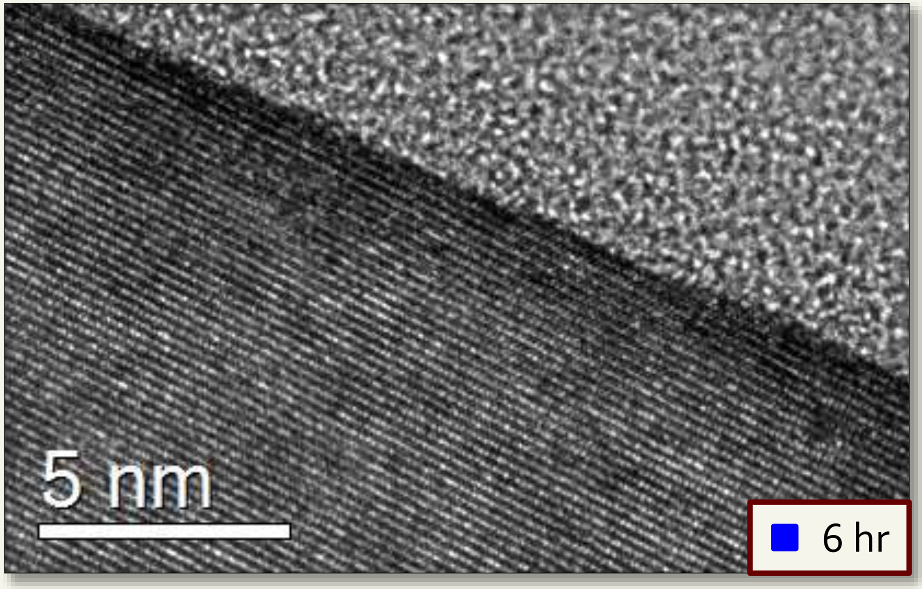


N$_2$P devices look very similar to NO Si and C-face images

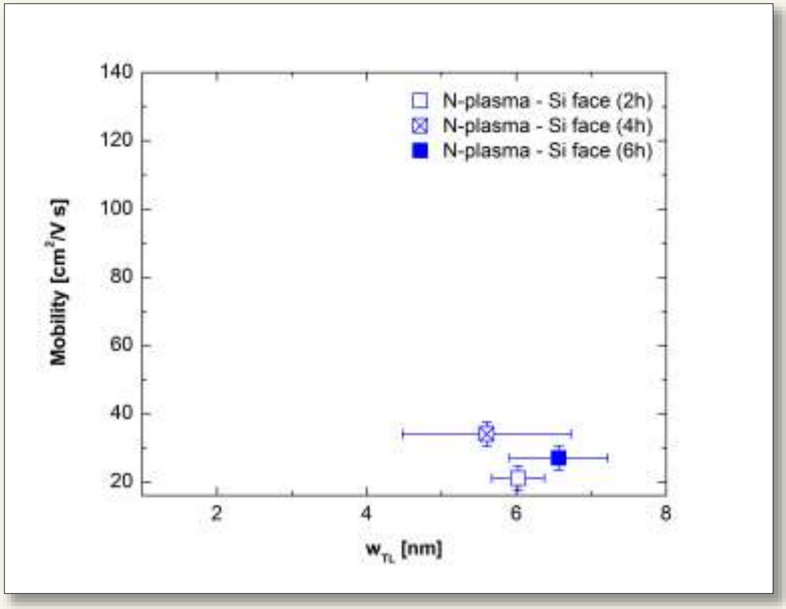


Very similar interface appearance and roughness characteristics

N2P anneal

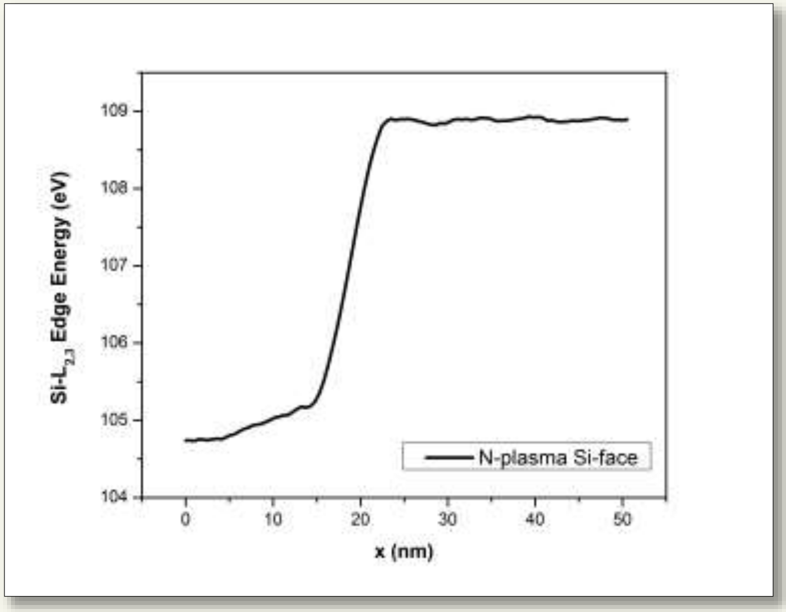


6hr annealed sample looks very similar to the others

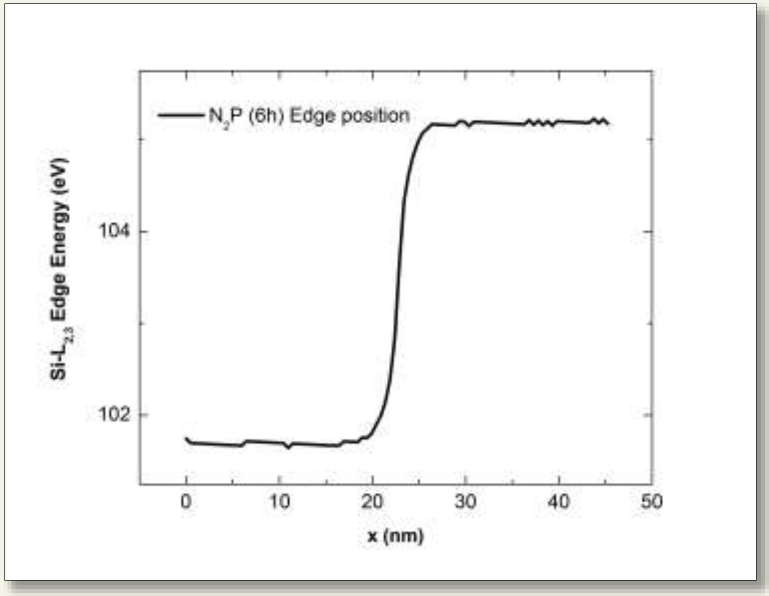


Chemical shift measurements reveal larger w_{TL} that agree with low μ

Update to results from EMC



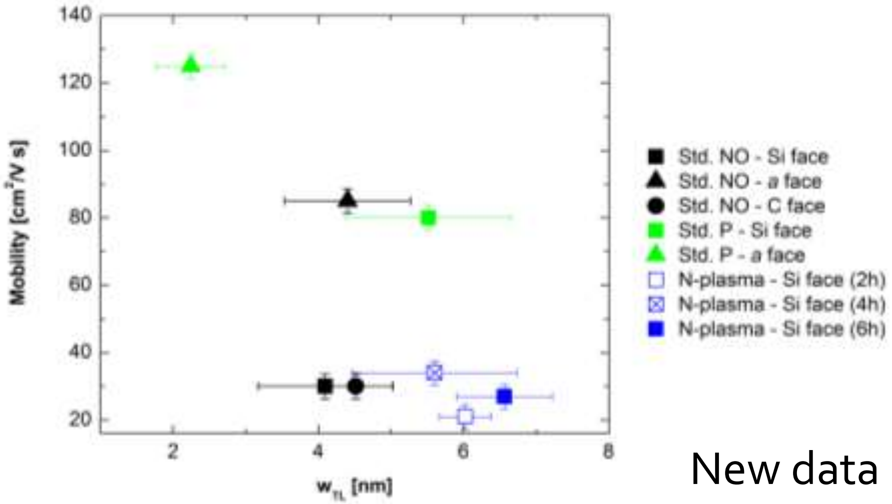
Asymmetric shift observed in 6hr N_2P sample in ***preliminary*** data



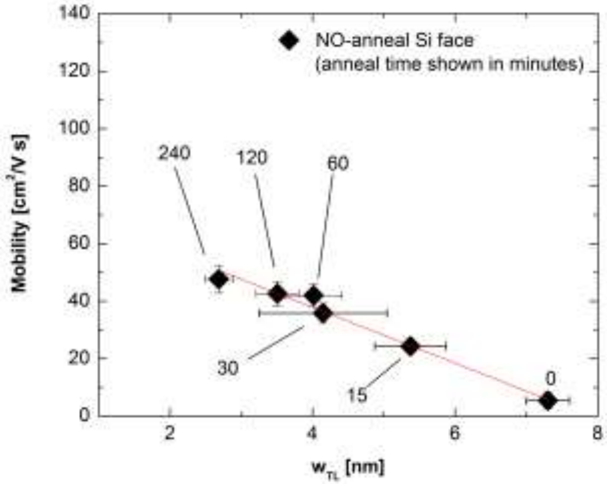
Typical shift observed in 6hr N_2P sample in ***current results***

Conclusions

- NO, P, & N-plasma samples:
  - Large variation in μ and w_{TL}
  - Less obvious trend than NO annealed samples alone
  - a-face and P-anneal samples have higher μ
  - Lower roughness does not guarantee smaller w_{TL} (when considering C-face sample)
  - Seem to have two distinct regimes, with similar but distinct relationships
    - More data needed to confirm this
  - Need to investigate fine structure in more detail to gain additional insight



New data



Previous NO data

Conclusions

- NO, P, & N-plasma samples:
  - Large variation in μ and w_{TL}
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  - *a*-face and P-anneal samples have higher μ
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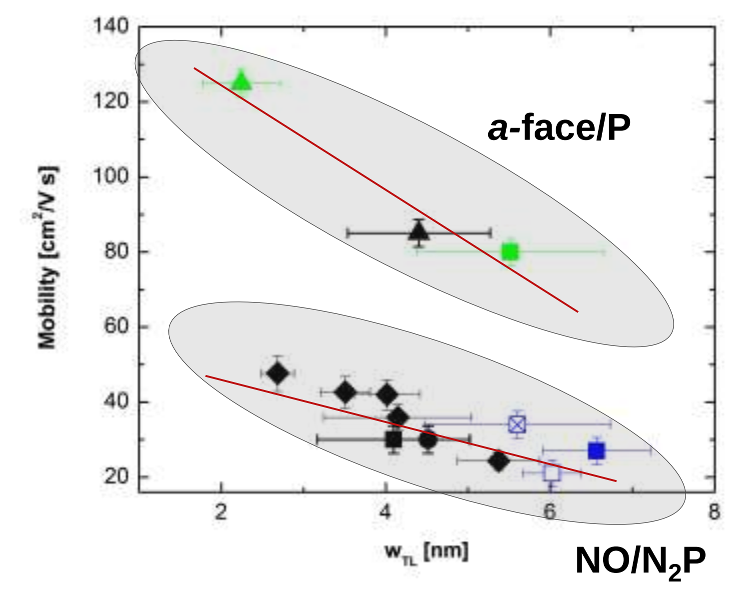
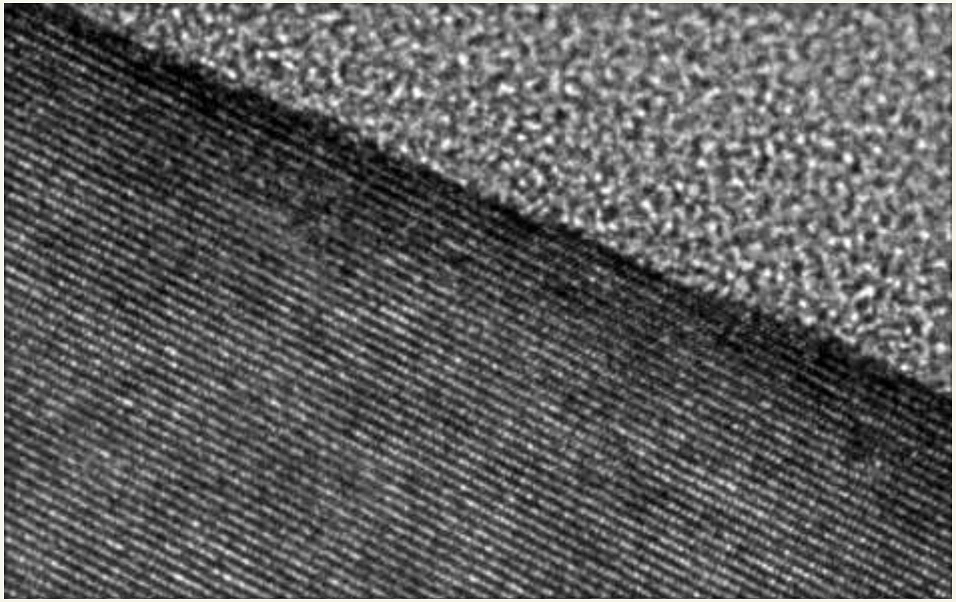


FUTURE WORK

Roughness from HRTEM reconstructions



$$G(\boldsymbol{u}) = T(\boldsymbol{u})F(\boldsymbol{u})$$

$$G(\boldsymbol{u}) = A(\boldsymbol{u})E(\boldsymbol{u})2\sin\chi(\boldsymbol{u})\,F(\boldsymbol{u})$$

$$\chi(u,\Delta f) = \pi(\boldsymbol{\Delta f})\lambda u^2 + \frac{1}{2}\pi C_s\lambda^3 u^4$$

- Roughness of interface can be used to calculate power spectrum of interface
  - Estimation of surface scattering-limited mobility possible from this [1,2]
- How to measure?
  - Difficult to digitize based on single image
  - HRTEM focal series reconstruction allows extraction of pure wave function phase
  - Could also accomplish this through electron holography

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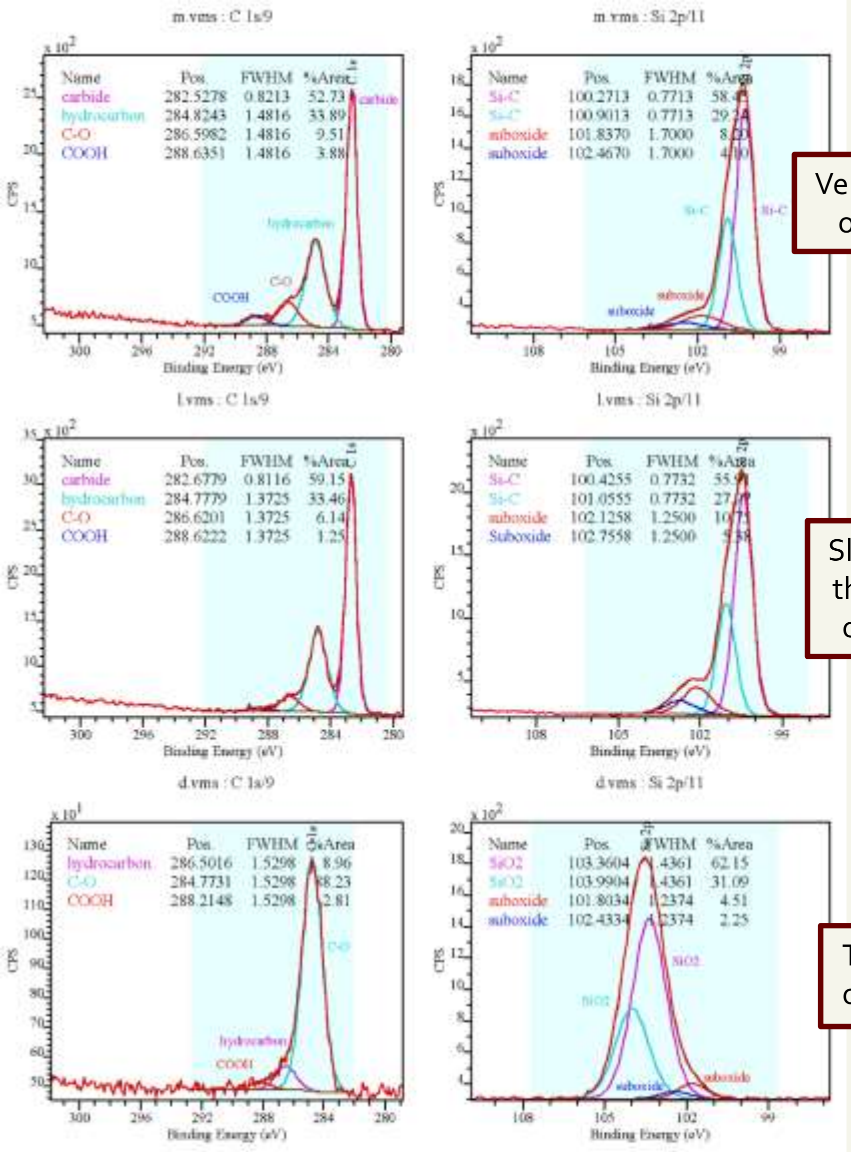
[1] Goodnick, S., *et al.*, Physical Review B, **32**, 8171–8186 (1985).

[2] Zhao, Y., *et al.*, IEEE Electron Device Letters, **30**, 987–989 (2009).

XPS depth profiles

- Motivation:
  - Suboxide states observed in slow oxide growth
  - 4H-SiC substrate heat treated at 1600°C for weeks under N_2 ambient
  - Unintentional slow oxidation from residual O_2



m.vms : C 1s/9

Name	Pos.	FWHM	%Area
carbide	282.5278	0.8213	52.73
hydrocarbon	284.8243	1.4816	33.89
C-O	286.5982	1.4816	9.51
COOH	288.6351	1.4816	3.88

m.vms : Si 2p/11

Name	Pos.	FWHM	%Area
Si-C	100.2713	0.7713	58.4
Si-C	100.9013	0.7713	29.24
suboxide	101.8370	1.7000	8.00
suboxide	102.4670	1.7000	4.10

Very thin oxide

l.vms : C 1s/9

Name	Pos.	FWHM	%Area
carbide	282.6779	0.8116	59.15
hydrocarbon	284.7779	1.3725	33.46
C-O	286.6201	1.3725	6.14
COOH	288.6222	1.3725	1.25

l.vms : Si 2p/11

Name	Pos.	FWHM	%Area
Si-C	100.4255	0.7732	55.9
Si-C	101.0555	0.7732	27.[illegible]
suboxide	102.1258	1.2500	10.73
Suboxide	102.7558	1.2500	5.88

Slightly thicker oxide

d.vms : C 1s/9

Name	Pos.	FWHM	%Area
hydrocarbon	286.5016	1.5298	8.96
C-O	284.7731	1.5298	88.23
COOH	288.2148	1.5208	2.81

d.vms : Si 2p/11

Name	Pos.	FWHM	%Area
SiO2	103.3604	1.4361	62.15
SiO2	103.9904	1.4361	31.09
suboxide	101.8034	1.2374	4.51
suboxide	102.4334	1.2374	2.25

Thick oxide

Data courtesy of K. Gaskell, L. Shahamat, and M. Al-Sheikhly

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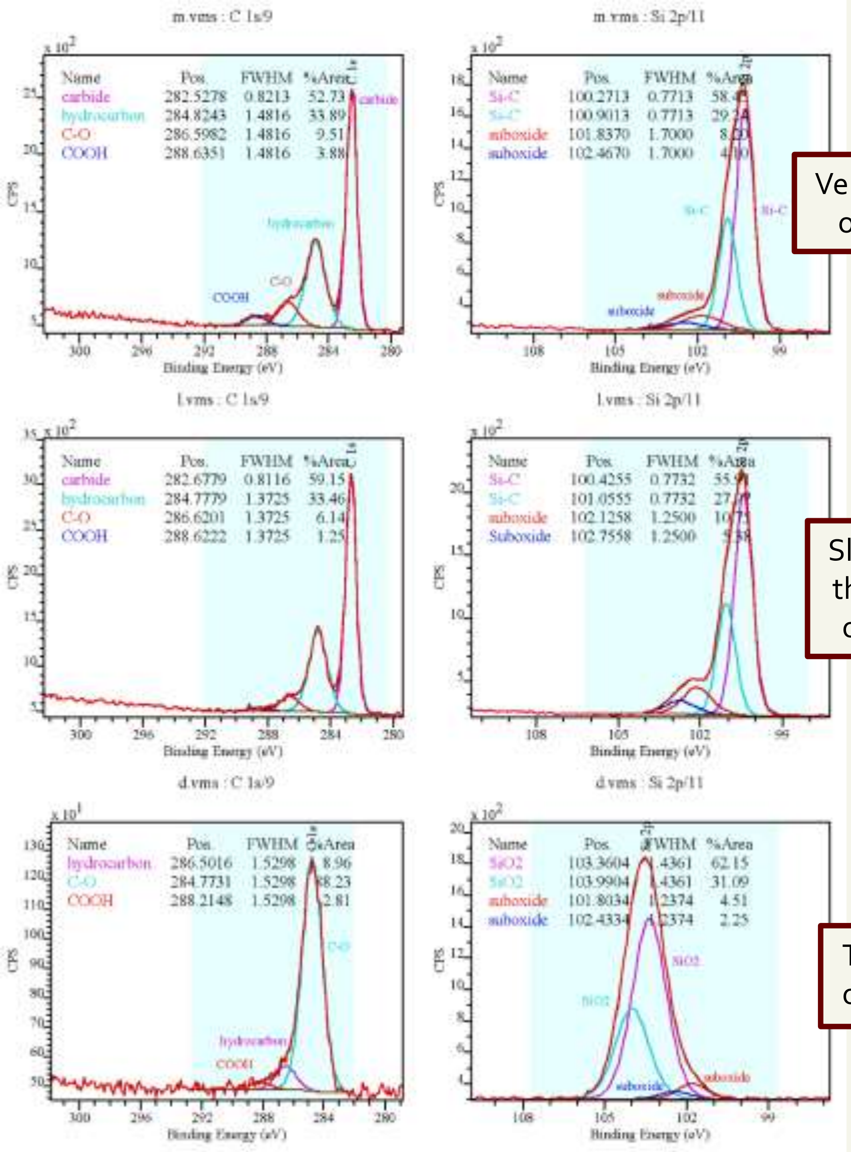
[1] Grunthaner, F. J. *et al.*, Journal of Vacuum Science and Technology, **16**, 1443 (1979)

XPS depth profiles

- "Spin-etch" depth profile to investigate native oxide of SiC in NO-annealed devices
  - Technique developed by Grunthaner *et al.* to investigate Si/SiO$_2$



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Suboxide	102.7558	1.2500	5.[illegible]

Slightly thicker oxide

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SiO2	103.9904	1.4361	31.09
suboxide	101.8034	1.2374	4.51
suboxide	102.4334	1.2374	2.25

Thick oxide

Data courtesy of K. Gaskell, L. Shahamat, and M. Al-Sheikhly

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[1] Grunthaner, F. J. *et al.*, Journal of Vacuum Science and Technology, **16**, 1443 (1979)

Acknowledgements

- ARL Contracts W911NF-11-2-0044 and W911NF-07-2-0046.
- NSF Graduate Research Fellowship Grant DGE 1322106
- NISPLab at UMD – supported by NSF and MRSEC
- Dr. Joshua Schumacher at NIST

THANK YOU

Questions and comments?